Design of comparator using Memristors*

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***Abstract*—This paper delves into the cutting-edge realm of computational technology by exploring the extraordinary capabilities of memristor properties, namely Non-Volatile memory and In-Memory Computing. These properties hold the potential to significantly boost computational power while simultaneously reducing system overhead.To better understand the underlying dynamics, the study extensively analyzes different memristor models, including Linear, Non-Linear, Team, and VTeam. Among these models, the VTeam stands out with remarkable performance advantages, making it the preferred choice for the implementation of basic gates like AND, NOT, and OR. Furthermore, the project involves the construction of comparators using memristors, enabling the researchers to evaluate and quantify the performance improvements. The simulations, conducted using the sophisticated Cadence tool and Verilog-A code, demonstrate a remarkable reduction in gate count and 86.9% better power dissipation and 62.9% better performance compared to traditional CMOS logic. These findings and discoveries presented in this research shed light on the immense potential of memristors, offering promising avenues for revolutionizing computational technology and pushing the boundaries of what's possible in the world of high-performance computing.**

***Index Terms*—CMOS.MOSFET,MRAM,MRL,SRAM,VTEAM**

I. Introduction

In the world of electronic circuits, three fundamental passive elements - the resistor, inductor, and capacitor - have long been the cornerstone of circuit design and functionality. However, the quest for more advanced and efficient computing components has led to the emergence of a revolutionary new element: the memristor. The memristor represents the final missing piece in the puzzle of electronic components and offers unprecedented possibilities for future technological advancements. The concept of a memristor was first proposed by Leon Chua in 1971, envisioning a unique two-terminal element whose resistance is determined by the magnitude, direction, and duration of the applied voltage. However, for decades, the memristor remained mostly a theoretical construct without concrete experimental evidence. It wasn't until 2008 when a breakthrough occurred at HP Labs, where researchers led by R. Stanley Williams demonstrated the first fabricated devices exhibiting true memristor characteristics.

Essentially, a memristor's defining feature lies in its ability to "remember" its most recent resistance state even after the voltage is turned off. This property of persistent memory makes memristors an extraordinary candidate for various applications in the field of electronics. The fabrication of memristors involves three crucial layers. The first and third layers consist of Titanium-Platinum bilayer electrodes, sandwiching the second layer, which comprises the active material Titanium dioxide (TiO2). This specific configuration allows for the dynamic behavior of the memristor, including the intriguing phenomenon of providing dynamical-negative resistance.

Memristors can be categorized into two main types based on their underlying principles: molecular and ionic thin film memristors and spin-based and magnetic memristors. The Titanium dioxide memristor model belongs to the former category. Other memristor models, such as Polymeric or Ionic memristors and Resonant tunneling diode memristors, also fall under this category. On the other hand, the second category of memristors includes Spintronic and STT-M memristors, showcasing diverse avenues of research and innovation in the field. In recent years, the demand for low-power devices has soared, primarily driven by the rapid expansion of CMOS technology. The pursuit of lower power consumption and smaller chip area has become a crucial challenge. Although not fully realized yet, memristors have started to emerge as a promising solution for non-volatile memory applications, offering impressive storage capacity compared to existing technologies.

This paper aims to explore the potential of memristors in modern electronic circuits, with a particular focus on their design, performance analysis, and application in combinational circuits. Designing a memristor cell using Verilog-A code in Cadence and conducting a thorough performance analysis to understand its behavior and characteristics, Implementing and designing combinational circuits using the built memristor block to explore their utility and efficiency in practical circuitry and creating and analyzing the performance of a magnitude comparator, which will serve as a case study for understanding the capabilities and limitations of memristors in various circuit applications.Throughout this ambitious project, we aim to uncover the full potential of memristors as a transformative element in the realm of electronic circuits, paving the way for innovative solutions that push the boundaries of computation, memory, and power efficiency. The journey of

exploring memristors promises exciting possibilities and holds the key to revolutionizing modern chip technologies and neural networks for a more advanced and interconnected future.

II. Memrister modeling

A. Fundamental properties

In the ever-evolving landscape of electronics, a remarkable addition has been made to the repertoire of passive elements - the memristor. Unlike its counterparts, the resistor, inductor, and capacitor, the memristor introduces an array of novel properties that promise to redefine the very fabric of electronic circuits. This deep dive into the nature of memristors unveils their extraordinary characteristics, encompassing dynamic negative resistance, pinched hysteresis, and non-volatile behavior, and elucidates their potential to revolutionize the future of computing and memory.

The heart of the memristor lies in its dynamic negative resistance - a property that sets it apart from conventional passive elements. Unlike traditional resistors, whose resistance remains constant, the memristor's resistance can vary significantly based on the magnitude, direction, and duration of the applied voltage. This unique attribute is rooted in the memristor's structure, featuring regions with varying doping levels. The interplay of these regions allows the memristor to dynamically change its resistance, giving rise to the captivating phenomenon of dynamic negative resistance. As voltage pulses surge through the memristor, its resistance dances fluidly, introducing a harmonious variability that holds great promise in diverse electronic applications.

In the symphony of memristor behavior, pinched hysteresis takes center stage. This captivating effect emerges when the memristor's response to a current source differs from its response to a voltage source. When a memristor is connected to a current source, it operates in a charge-controlled mode, presenting itself with a characteristic memristance of one ohm. However, the melodic transformation unfolds when the memristor is connected to a voltage source. In this flux-controlled mode, the memristor assumes a memductance of one mho. This intriguing interplay between flux and charge adds a rich tonality to the memristor's performance, rendering it a versatile component for diverse electronic orchestrations.

The allure of memristors extends to their non-volatile behavior - an enchanting quality that endows them with the ability to retain their state even after the power supply is disconnected. When charge flow is interrupted, the memristor embraces its last memristance value, akin to a persistent memory. This captivating feature holds profound implications for memory storage applications, as it allows memristors to safeguard data against power interruptions, like a timeless melody preserved in silence, waiting to be reawakened.

The unique and mesmerizing nature of memristors has sparked an aria of possibilities in the world of electronics. Their dynamic negative resistance, pinched hysteresis, and non-volatile behavior combine to form a symphony of capabilities that resonates across diverse applications.

In memory storage, memristors present an opportunity to revolutionize the landscape. As the quest for higher density, lower power consumption, and faster access times in memory technology intensifies, memristors emerge as promising contenders. Their non-volatile nature offers a compelling solution to address the challenges faced by conventional memory technologies, with the potential to unleash a crescendo of advancements in data storage.

B. Types of memritor

Memristors, the intriguing fourth fundamental passive element, come in various types, each showcasing distinct mechanisms and properties. Here, we explore different categories of memristors and their fascinating characteristics.

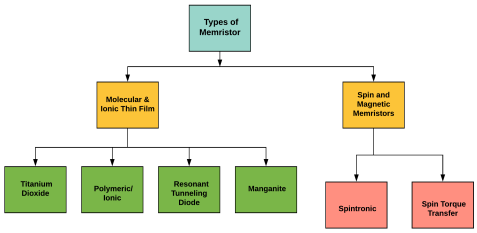


Fig 1. Types of memristers

1. Molecular and Ionic Thin Film Memristive Systems

a) Titanium Dioxide Memristors: Developed at HP Labs, these memristors feature a two-layer thin "sandwich" of titanium dioxide films. The atomic structure of the memristor undergoes a state change as the motion of atoms in the films aligns with the movement of electrons in the material. The resistance alteration occurs through the migration of oxygen vacancies between the layers, enabled by crossbars of nanowires passing charges through.

b)Polymeric (Ionic) Memristors: These memristors explore dynamic doping of polymer and inorganic dielectric materials, leading to hysteresis-like behaviors. A single passive layer between an electrode and an active thin film encourages the extraction of ions from the electrode, provoking memristive effects.

c)Manganite Memristive Systems: Utilizing bilayer oxide films based on manganite, these systems were discovered to exhibit memristive properties, offering an alternative to titanium dioxide-based memristors.

d)Resonant-Tunneling Diode Memristors: Certain types of quantum-well diodes with specific doping designs between the source and drain regions display memristive properties.

2. Spin-Based and Magnetic Memristive Systems

a)Spintronic Memristors: Under development by various labs, including Seagate, these magnetic memristors rely on electron spin polarization alteration. The resistance state changes based on the movement of a magnetic "domain" wall that separates polarities, resulting in hysteresis-like behavior.

b)Spin Torque Transfer (STT) MRAM: In some cases, Non-Volatile Magnetic Random Access Memory (NIRAM) bits exhibit memristive properties. Spin valve configurations in certain MRAM bits rely on a spin torque induced by

current flowing through a magnetic junction, affecting the difference in spin orientation between the two sides of the junction. Depending on the materials used, these spin torque constructions can display both ionic and magnetic properties, often referred to as ”second-order memristive systems.”

Each type of memristor holds immense potential for diverse applications. Molecular and ionic thin film memristors offer promise in memory and computing, while spin-based and magnetic memristors pave the way for advanced magnetic memory and spintronic devices. The dynamic interplay between these various memristor types sets the stage for revolutionary advancements in the realm of electronics, promising a symphony of possibilities in memory storage, computing, and neuromorphic engineering. As researchers continue their quest to unlock the full potential of these extraordinary elements, the symphony of memristors plays on, heralding a future of innovation and transformative technologies.

C. Logic operation

a)Imply logic: Aside from the well-known fundamental logic operations— AND, OR, and NOT implication logic is another operation proposed. It is also known as imply. The symbol of IMPLY gate is denoted as ”-”. When x is true (1) but y is false (0), x-y is false (0). For the other cases, x—y is always true. Hence, x-y is logically equivalent to x+y. The functions of input memristor and working memristor are described as input memristor and working memristor. Input memristor(p)is a memristor that holds an input signal and stays its resistance state after computation. Working memristor(q) is a memristor that can hold an input signal, a constant O value, or the operational result of an IMPLY gate. Case 1: If the memristor p is in logic ”1” which means it is in the low-resistance state (closed) and Vp is approximate to Vcond, a voltage drop (Vset Vcond) will be across the memristor q. Hence, this voltage drop on the memristor q is negative this will not cause the memristor q change its state. The corresponding Boolean expression of this operation is as follows: 10=1, p’+q =q. Case 2: If the memristor p is in logic ”O” which means it is in the high-resistance state (open) and Vp is approximate to 0, a voltage drop Vset will be across the memristor(q). Hence, the resistance state of memristor q will be changed from high to low. The result of this case is logic ”1” and saved on the memristor q. The corresponding Boolean expression of this operation is as follows: p=0, p’+q =1.

b)MRL-Memrister ratioed logic: Both AND and OR logic gates consist of two memristors connected in series with opposite polarity, as shown in Fig.3(a,b). The only difference between the two gates consists in the polarity of the memristors with respect to where the inputs are applied. The output node is the common node of the connected memristors, whereas each input signal is applied to the floating terminal of every memristor. Both logic gates react similarly to identical inputs (both being either logic ’1’ or logic Since the voltage drop between inputs is zero, the voltage at the output node follows the input voltage.

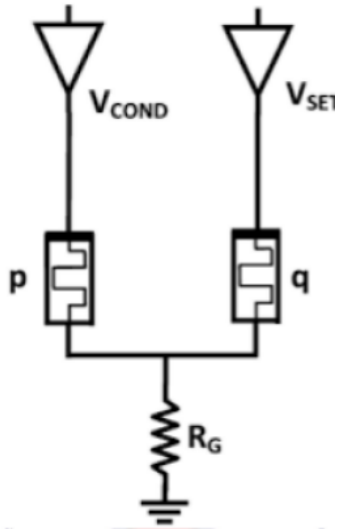


Fig. 1. Imply logic

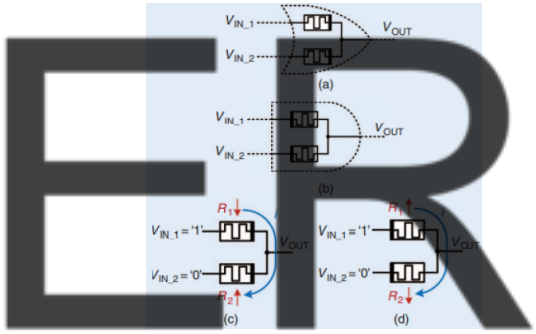


Fig 3. MRL

However, when the inputs are different there is current flowing from the high voltage terminal (where the ’1’ is applied) to the grounded terminal (where the ’O’ is applied), thus potentially affecting the memristance of the devices.This case is shown in Fig.3(c) for an OR logic gate. Assuming initially RI=OFF and R2=ON , at the end of the computational process the memristors have changed their initial states. For the AND logic gate the different polarities have as a result the state of each memristor to switch in the opposite manner.

D. Different models of memristor

1.Linear Ion Drift Model: The linear ion drift model involves two memristors connected in series. One memristor is completely oxidized titanium, acting as the positive terminal with high conductance. The other memristor has titanium with extra holes, leading to low conductance. This model assumes average electronic mobility and conductivity. Its voltage range typically lies between -2 to +2 volts. The model assumes free movement of oxygen vacancies along the entire length of the memristor, without any hindrance from boundary conditions,

making it relatively easy to implement with closed-form solutions.

2.Non-Linear Ion Drift Model: In the non-linear ion drift model, a voltage-controlled memristor is assumed, where the voltage and internal state derivative exhibit a non-linear dependency. This model also considers asymmetric switching behavior. While the linear drift model produces hysteresis characteristics, it may lack accuracy in certain scenarios, especially for applications like logic circuits, where non-linear characteristics are needed.

3.Simons Tunnel Barrier Model: The Simon's Tunnel Barrier Model is a more accurate physical representation of memristors. Unlike previous models, it uses a resistor asynchronous with an electron tunnel barrier. It employs hyperbolic and exponential functions to model electron tunneling. This model is highly accurate but more complex in design and primarily used for specific purposes due to its intricacies.

4.TEAM Model (Threshold Adaptive Memristor): The TEAM model, presented by Kvatinsky et al., is a simple and general model based on the Simmons tunnel barrier model. It involves assumptions for analysis simplification and computational efficiency. Below a specific threshold, the state variable remains unchanged. Instead of exponential dependence, a polynomial dependence represents the memristor current and internal state drift derivative. The TEAM model is accurate enough with a mean error of 0.2% and significantly boosts simulation runtime efficiency by 47.5%, meeting the requirements of memristive systems.

5.VTEAM Model (Voltage Threshold Adaptive Memristor): The VTEAM model is an extension of the Threshold Adaptive Memristor (TEAM) model and is designed to describe voltage-controlled memristors. Like the TEAM model, it is simple, general, and flexible, capable of characterizing different voltage-controlled memristors. The VTEAM model exhibits a relative root-mean-square error of 1.5% and remains computationally efficient compared to existing memristor models. Each of these models offers unique advantages and serves specific purposes in memristor simulations and applications. Understanding and utilizing these models enables researchers and engineers to exploit the full potential of memristors in advancing electronic circuits, memory systems, and emerging computing technologies.

III. Logic implementation

A. NOT gate

A logical inverter, sometimes called a NOT gate to differentiate it from other types of electronic inverter devices, has only one input.

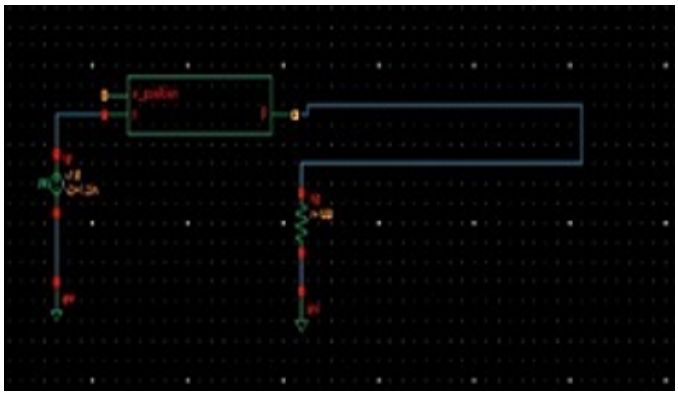


Fig 4. NOT gate

It reverses the logic state.lf and only if the input does not reach state 1, the output of a NOT Gate reaches state I. Logic circuit for NOT gate if given in fig 4.

B. AND gate

The AND gate is so named because, if O is called false" and 1 is called "true," the gate acts in the same way as the logical and" operator. The fg 5 show the circuit symbol logic combinations for an AND gate. It has one output and n inputs The output is "true" when both inputs are "true." Otherwise, the output is "false." In other words, for 2 bit and the output is '1' only when both inputs one AND two are '1' else output is '0'.

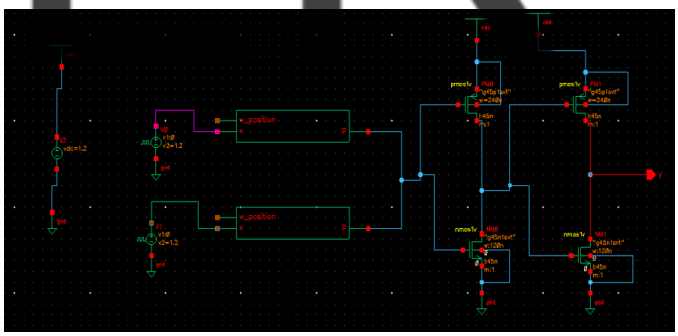


Fig 5. AND gate

C. OR gate

It's a digital circuit with two or more inputs that creates an output that's the logical OR of all those inputs. The fig 6 show the circuit symbol and logic combinations for an Or gate. It has one output and n inputs (n 2). The output of the 2-bit OR gate is low if both of its inputs are low. Which means whenever the inputs are '0','0' output will be 'O', Otherwise output will be '1'.

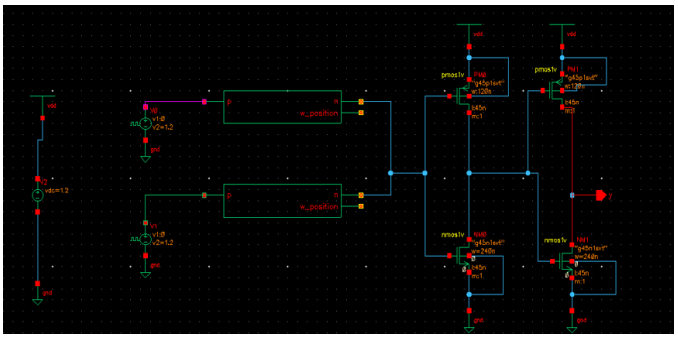


Fig 6. OR gate

D. 1-bit comparator

The Digital Comparator is used to compare the value of two binary digits. A comparator used to compare two bits is called a single bit comparator. We logically design a circuit for which we will have two inputs one for A and another for B and have three output terminals, one for A greater than B condition, one for A=B condition and one for A less than B condition.

A	B	A greater than B	A=B	Aless than B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

From the above truth table logical expressions for each output can be expressed as A greater than B=AB', A less than B=A'B, (A=B)=A'B'+AB. The corresponding circuit is provided in fig 7

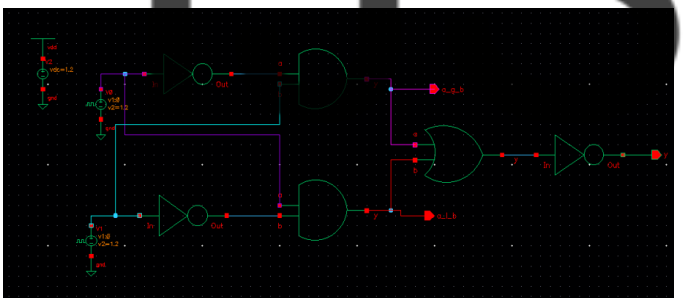


Fig 7. 1-Bit comparator

E. 2-bit copmarator

A magnitude digital Comparator is a combinational circuit that compares two digital or binary numbers in order to find out whether one binary number is equal, less than or greater than the other binary number. A comparator used to compare two binary numbers each of two bits is called a 2-bit Magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to, and greater than between two binary numbers.

A>B:A1B1' + A0B1'B0' + A1A0B0'
A=B: (A0 Ex-Nor B0) (A1 Ex-Nor B1)
A<B:A1'B1 + A0'B1B0 + A1'A0'B0

In A less than B Circuit(fig 8) A1 and Bl are compared, if A1 less than B1 and if A1=B1 then A0 and B0 are compared if A0 less than B then the output will be '1' else output will be same thing is indicated in equation.

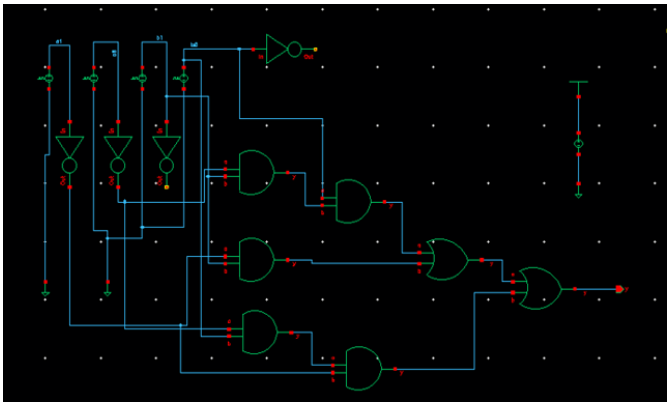


Fig 8. A less than B

In A greater than B Circuit(fig 9) A1 and Bl are compared, if A1 is greater than B1 and if A1=B1 then A0 and B0 are compared if A0 is greater than B0 then the output will be '1' else output will be '0'. same thing is indicated in equation.

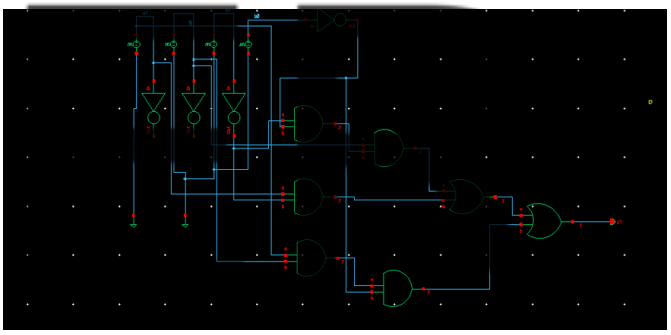


Fig 9. A greater than B

The circuit in fig 10 both A greater than B and A less than B are implemented by which A=B logic is found by ex-nor operation. The Ex-Nor operation is done using basic gates Which are shown in the same circuit.

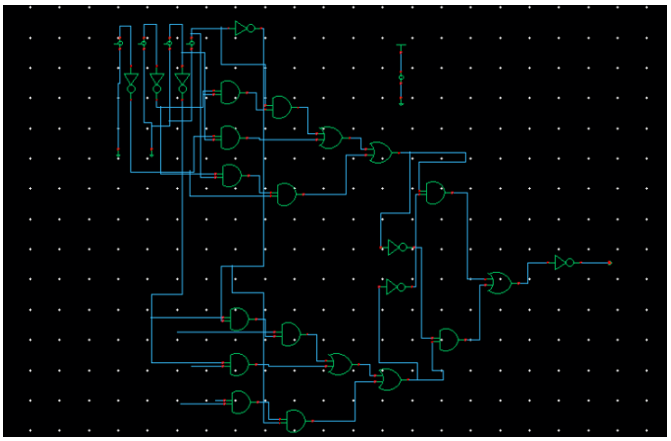


Fig 10. A=B

IV. Results and Discussions

A. Results of NOT gate

NOT gate specifications:
Input: Vpulse V1=1V
Time Period : 40ns
Pulse Width :20ns

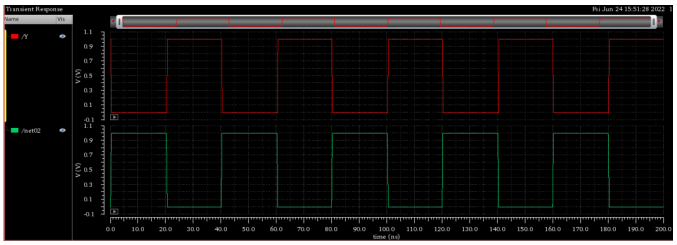


Fig 11. NOT gate results

When the input is high the NOT gate inverse the voltage to give output zero and when the input is low the NOT gate inverse the output to give output one.

B. Results of AND gate

AND gate specifications:
Input: Vpulse VI,V2=1V
V1 Time Period : 40ns
V2 Time Period : 20ns
V1 Pulse Width : 20ns
V2 Pulse Width : 10ns

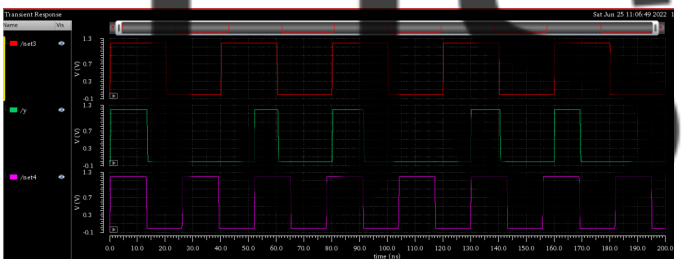


Fig 12. AND gate results

When both the inputs are low the output is zero. When either of the one input is low the output is zero whereas when both the inputs are high the output is one.

C. Results of OR gate

OR gate specifications:
Input: Vpulse VI,V2=1V
V1 Time Period : 40ns
V2 Time Period : 20ns
V1 Pulse Width : 20ns
V2 Pulse Width : 10ns

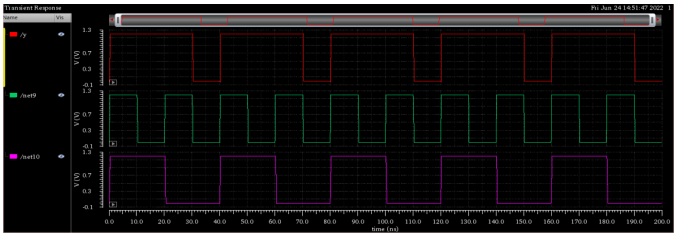


Fig 13. OR gate results

When both the inputs are low the output is zero. When either of the one input is high the output is one also when both the inputs are high the output is one.

D. Results of 1-bit comparator

One bit comparator specifications: Input: Vpulse VI,V2=1V
V1 Time Period : 40ns
V2 Time Period : 20ns
V1 Pulse Width : 20ns
V2 Pulse Width : l0ns

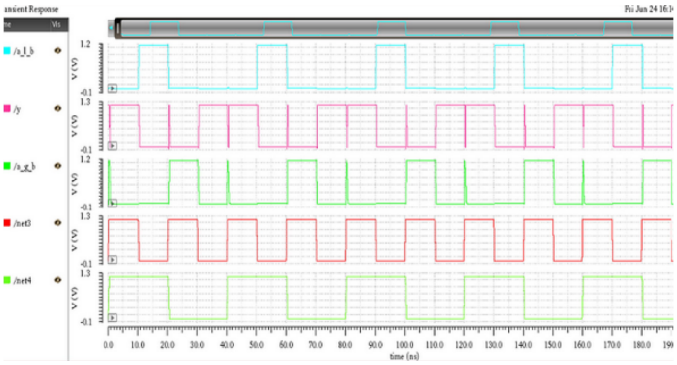


Fig 14. 1-bit comparator results

When both the inputs are low or high the output is one for A+B.When net3 in Figure 14 is high and net4 in Figure 14 is low then the output is one for A greater than B. When net3 in Figure 14 is low and net4 in Figure 14 is high the output was on3 for A less than B.

E. Results of 2-bit comparator

Two bit comparator specifications:
Input: Vpulse V1,V2,V3,V4=1V
V1 Time Period : 20ns
V2 Time Period : 40ns
V3 Time Period : 60ns
V4 Time Period : 80ns
V1 Pulse Width : 10ns
V2 Pulse Width : 20ns
v3 Pulse Width : 30ns
V4 Pulse Width : 40ns

Fig 15. A=B

When the msb and lsb of both the inputs are equal then the A equal to B output was one.

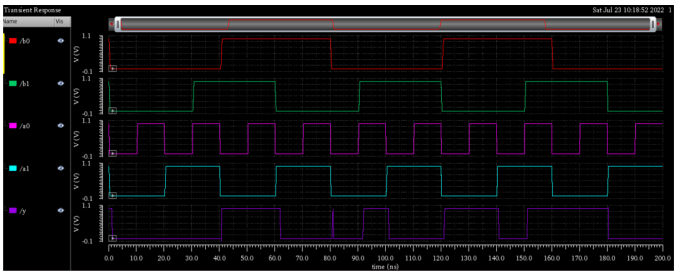
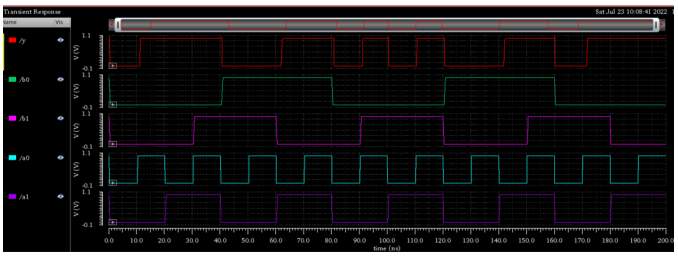


Fig 16. A less than B

When msb of first input was lesser than msb of second input or when msb of both inputs were equal and if lsb of input one is less than lsb of second input then the output is one.



A greater than B

When msb of first input was greater than msb of second input or when msb of both inputs were equal and if lsb of input one is greater than lsb of second input then the output is one.
A comparison of power dissipation and propagation delay for AND circuit and 2-bit comparator circuit using CMOS and memristor is shown in the table below

CMOS(AND)[12]	Memristor(AND)	CMOS(2-bit comparator)[12]	Memristor(2-bit comparator)
Pd=0.119ns	0.062ns	1.46ns	0.541ns
Power=3.1uW	1.76uW	233.98uW	30.61uW

Table 1

It is observed that the memristor circuit consumes 86.9% less power than the conventional CMOS circuit and the propagation delay is 62.9% less than CMOS circuit. Thus memristor circuit has better performance and power consumption.

V. Conclusion

The basics properties of memristor like non-volatile property, dynamic negative resistance, pinched hystersis are explored and then different types of memristors are also studied. Some Logics of memristor such as imply, MIRL are used to make memristor basic gates. The basic memristor model is built using Linear-ion and V team models. Since V team model gives more noise margin as compared to Linear-ion, Vteam is used for making basic gates. The basic gates such as NOT, AND, OR, NAND, NOR are built using Vteam memristor model and the logic used to implement it is MRL logic. Using these basic gates 1bit comparator and 2bit comparators are built and we analysed the results. The obtained models of 2-bit comparator and AND using Memristor uses less die space as compared to CMOS models. The propagation delay and power parameters of 2-bit comparator and AND gate using Memristor are compared with the CMOS models of 2-bit comparator and AND gates. The delay and power are reduced by half in the AND gate and whereas in 2-bit comparator the delay got reduced by half and the power got reduced drastically. Finally, the propagation delay comparison of AND gate with MOSFET reduced by 47% and the total power consumed by the AND gate reduced by 43.2%, The 2-bit comparator output propagation delay is reduced by 62.9% and total power consumed is reduced by 86.9% when compared to MOSFETs.

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